BK7257 Datasheet

DS-BK7257-E01 V1.0

2025/5/9

Contents

1. Features

Wi-Fi®

- IEEE 802.11b/g/n/ax 1x1 compliant
- 20 MHz and 40 MHz channel bandwidths for 2.4 GHz
- Supports downlink Multi-User Multiple-Input Multiple-Output (DL MU-MIMO)
- Supports Orthogonal Frequency Division Multiple Access (OFDMA)
- Supports Target Wake Time (TWT)
- TX and RX Low-Density Parity Check (LDPC) support for extended range
- WPA™/WPA2™/WPA3™-Personal support for enhanced security
- Supports STA and SoftAP modes
- Supports concurrent SoftAP + STA
- TX power up to +20 dBm
- RX sensitivity -98 dBm

Bluetooth® Low Energy

- Bluetooth Low Energy (LE) 5.4
- Supports Bluetooth Low Energy 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Supported Bluetooth Low Energy features: LE Audio, Angle of Arrival (AoA) and Angle of Departure (AoD) direction finding, 2 Mbps, advertising extensions, and long range
- Supports an antenna array with up to 16 antennas for precise positioning

Core

- Arm®v8-M STAR-MC1 MCU at up to 480 MHz:
  - Double-precision floating-point unit (FPU)
  - 16 KB ITCM + 16 KB DTCM
  - Embedded TrustZone®
  - Supports DSP instructions with SIMD
  - 3.84 CoreMark®/MHz
- UART flash download
- Serial Wire Debug (SWD) interface

Memories

- SiP flash (XIP): 4 MB or 8 MB
- 640 KB Share SRAM
- 64 KB ROM
- eFuse

Clock Management

- External oscillator: 26 MHz crystal oscillator (XTALH)
- Internal oscillators: 26–360 MHz digitally controlled oscillator (DCO), 32 kHz ring oscillator (ROSC)
- 320 MHz/480 MHz PLL (DPLL)
- Audio PLL (APLL)

Power Management

- 2.5 to 4.35 V VBAT supply
- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)
- Embedded buck (DC-DC) converter and LDO regulators
- Low power consumption:
  - Active mode RX: 17.5 mA
  - Sleep mode: 43 µA
  - Deep sleep mode: 16 µA
  - Shutdown mode: 2.5 µA

Peripherals

- 28 GPIOs
- 2x SPI
- 2x QSPI
- 3x UART, 1 with flash download support
- 1x Smart Card controller (SC)
- 1x SDIO
- 2x I2C
- 1x high-speed USB2.0 (HS)
- 1x LIN controller (LIN)
- 2x general-purpose DMA controller (GDMA), each with 8 channels
- 1x DMA2D controller (DMA2D)

- 1x rotation module (ROTT)
- 2x scaling module (SCALE)
- 1x JPEG hardware encoder
- 1x JPEG hardware decoder
- 1x 720p H.264 video encoder (H.264)
- 6x 32-bit PWM channel
- 1x I2S
- 1x four-band digital hardware equalizer (EQ)
- 2x audio ADC
- 1x audio DAC
- 1x SBC accelerator (SBC)
- 12-bit AUX ADC, up to 7 channels
- 6x 32-bit general-purpose timer
- 2x watchdog timer (WDT)
- 1x real-time counter (RTC)
- 1x IrDA
- 1x temperature sensor

Packaging

- QFN56 package, 7 x 7 mm
- Operating temperature range: -40 to +85 °C

Applications

- HMI (Human Machine Interface) applications
- Home appliance
  - Refrigerator
  - Air conditioner
  - Thermostat
  - Washing machine
  - Robot cleaner
- Smart plug
- Smart lighting
  - Light bulb

  - Light switch
  - Ceiling light
  - Stand light
- Others
  - Remote controller
  - Toy
  - Drone
  - Industrial terminal
  - Factory automation sensor/switch
  - Smart meter
  - Payment terminal
  - Industrial computer
  - Medical devices
  - Kitchen appliances
  - Home automation switch/sensor
  - Door lock
  - Door camera

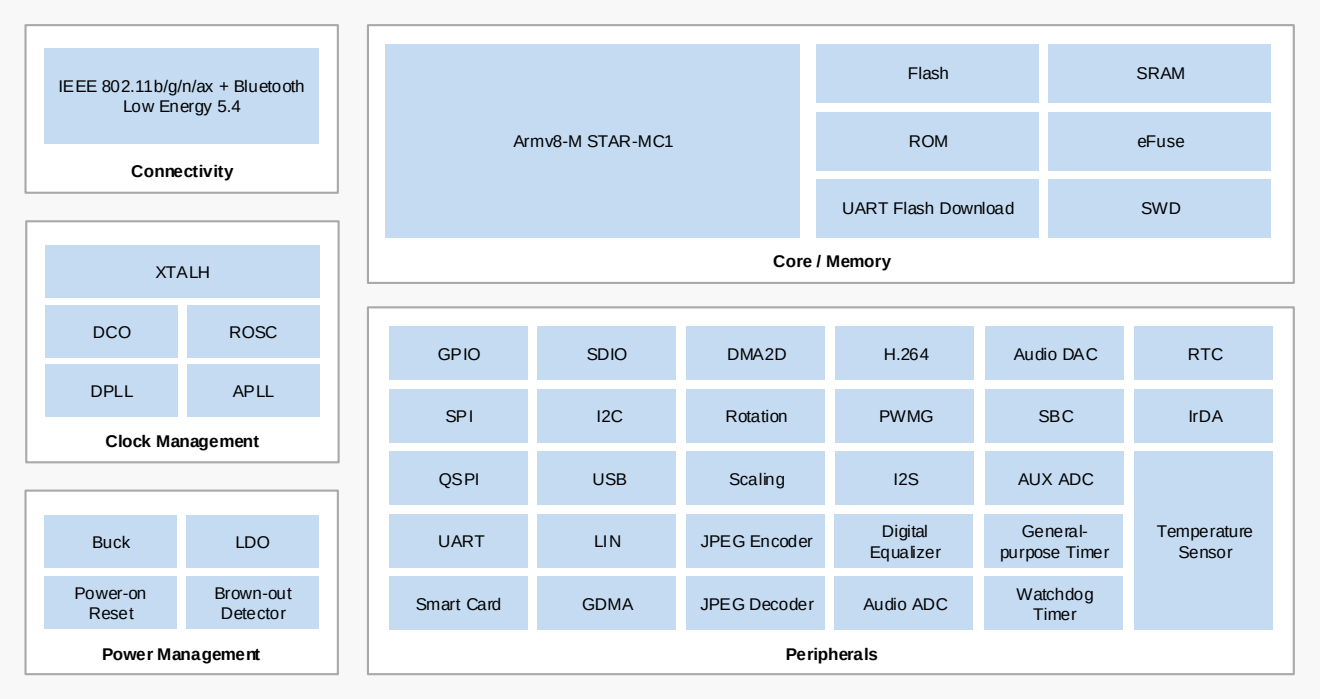
2. Overview

The BK7257 is a highly integrated 1x1 single-band 2.4 GHz Wi-Fi 6 (802.11b/g/n/ax) and Bluetooth Low Energy (LE) 5.4 combo solution designed for applications that require abundant resources and low power consumption. The integration of a 32-bit Armv8-M STAR-MC1 MCU and a comprehensive set of peripherals makes the BK7257 ideal for advanced Internet of Things (IoT) applications.

Using advanced design techniques and ultra-low power process technology, the BK7257 delivers high integration and minimal power consumption for IP cameras, HMI applications, smart locks, and other advanced IoT applications.

Figure 2-1 shows the general block diagram of the BK7257.

Figure 2-1 BK7257 Block Diagram



3. Pin Descriptions

The BK7257 provides Wi-Fi and Bluetooth LE functionality in a 7 x 7 mm, 56-pin QFN package.

3.1 QFN56 Pin Descriptions

Figure 3-1 shows the pin assignments of the QFN56 package.

Figure 3-1 QFN56 Pin Assignments

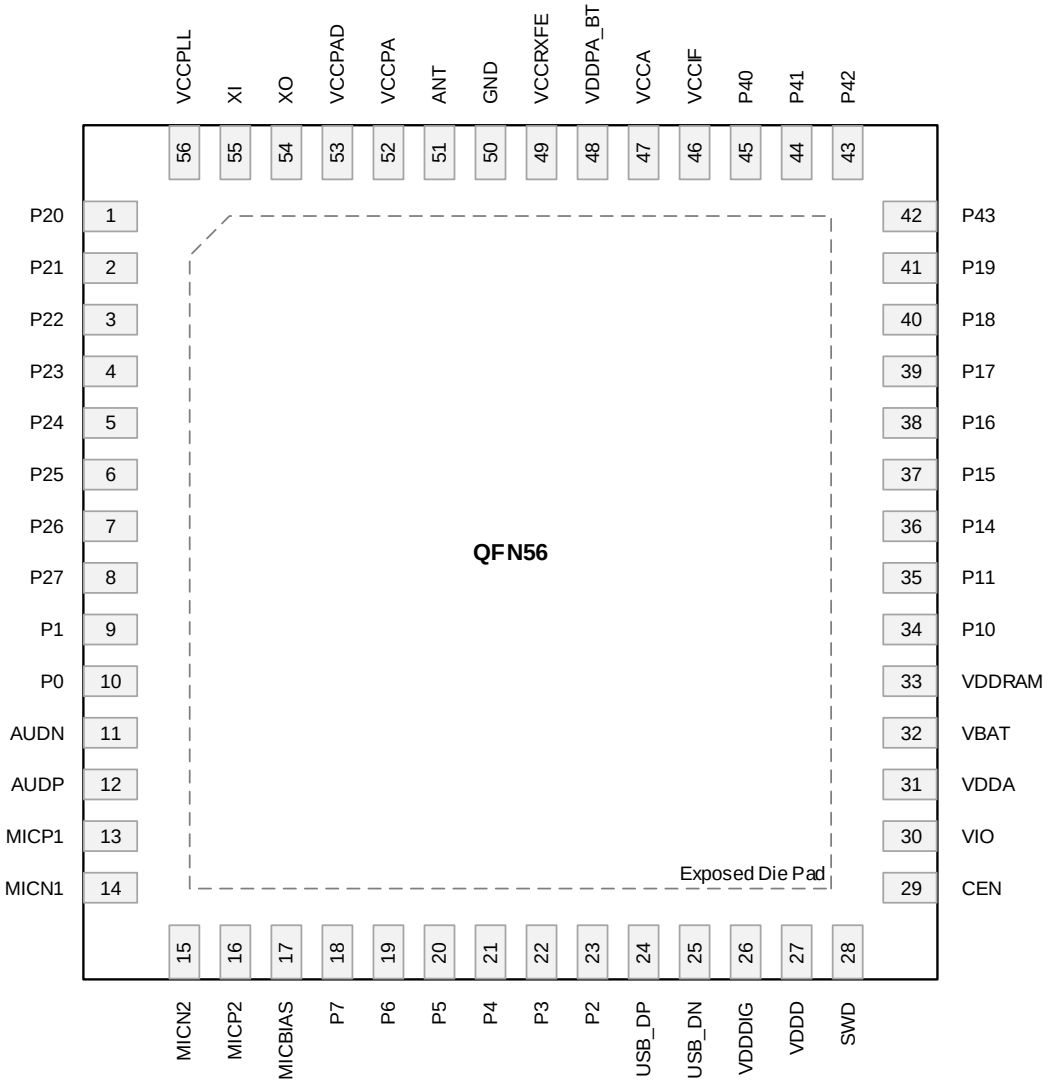


Table 3-1 shows the pin descriptions of the QFN56 package.

Table 3-1 QFN56 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	P20	I/O	Digital	• GPIO20: general-purpose I/O • I2C0_SCL: serial clock • SWCLK: serial wire clock
2	P21	I/O	Digital/Analog	• GPIO21: general-purpose I/O • I2C0_SDA: serial data • SWDIO: serial wire data • ADC6: analog input channel
3	P22	I/O	Digital/Analog	• GPIO22: general-purpose I/O • CLK26M: 26 MHz clock output • PWMG0_PWM2: PWM2 channel of PWMG0 • ADC5: analog input channel • QSPI0_SCK: serial clock
4	P23	I/O	Digital/Analog	• GPIO23: general-purpose I/O • PWMG0_PWM3: PWM3 channel of PWMG0 • ADC3: analog input channel • QSPI0_CS: chip select
5	P24	I/O	Digital/Analog	• GPIO24: general-purpose I/O • LPO_CLK: 32 kHz clock output • PWMG0_PWM4: PWM4 channel of PWMG0 • ADC2: analog input channel • QSPI0_IO0: data
6	P25	I/O	Digital/Analog	• GPIO25: general-purpose I/O • IRDA: infrared data • PWMG0_PWM5: PWM5 channel of PWMG0 • ADC1: analog input channel • QSPI0_IO1: data
7	P26	I/O	Digital	• GPIO26: general-purpose I/O • QSPI0_IO2: data
8	P27	I/O	Digital	• GPIO27: general-purpose I/O

Pin #	Name	I/O	Type	Description
				• CIS_MCLK: master clock • CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M) • QSPI0_IO3: data
9	P1	I/O	Digital/Analog	• GPIO1: general-purpose I/O • UART1_RX: receive data input • I2C1_SDA: serial data • SWDIO: serial wire data • SC_CLK: clock • ADC13: analog input channel • LIN_RXD: receive data input
10	P0	I/O	Digital/Analog	• GPIO0: general-purpose I/O • UART1_TX: transmit data output • I2C1_SCL: serial clock • SWCLK: serial wire clock • SC_IO: data input/output • ADC12: analog input channel • LIN_TXD: transmit data output
11	AUDN	-	Analog output	Audio channel negative output
12	AUDP	-	Analog output	Audio channel positive output
13	MICP1	-	Analog input	Microphone 1 positive input
14	MICN1	-	Analog input	Microphone 1 negative input
15	MICN2	-	Analog input	Microphone 2 negative input
16	MICP2	-	Analog input	Microphone 2 positive input
17	MICBIAS	-	Analog output	Microphone bias output
18	P7	I/O	Digital	• GPIO7: general-purpose I/O • PWMG0_PWM1: PWM1 channel of PWMG0 • QSPI1_IO3: data
19	P6	I/O	Digital	• GPIO6: general-purpose I/O • CLK13M: 26 MHz clock output (divide by 1/2/4/8) • PWMG0_PWM0: PWM0 channel of

Pin #	Name	I/O	Type	Description
				PWMG0 • QSPI1_IO2: data
20	P5	I/O	Digital	• GPIO5: general-purpose I/O • SPI1_MISO: master in slave out • SDIO_DATA1: data • QSPI1_IO1: data
21	P4	I/O	Digital	• GPIO4: general-purpose I/O • SPI1_MOSI: master out slave in • SDIO_DATA0: data • QSPI1_IO0: data
22	P3	I/O	Digital	• GPIO3: general-purpose I/O • SPI1_CSN: chip select • SDIO_CMD: command/response • SC_VCC: power supply to the smart card • QSPI1_CS: chip select
23	P2	I/O	Digital	• GPIO2: general-purpose I/O • SPI1_SCK: serial clock • SDIO_CLK: clock • SC_RSTN: reset • LIN_SLEEP: transceiver sleep mode (active low) • QSPI1_SCK: serial clock
24	USB_DP	I/O	Digital	USB D+
25	USB_DN	I/O	Digital	USB D-
26	VDDDIG	-	Analog output	Digital core LDO output
27	VDDD	-	Analog output	Digital buck/LDO output
28	SWD	-	Analog output	Digital buck switch output
29	CEN	-	Analog input	Chip enable, active high
30	VIO	-	Analog output	IO LDO output
31	VDDA	-	Analog output	Analog LDO output
32	VBAT	-	Power	Chip power supply
33	VDDRAM	-	Analog output	EXMEM LDO output

Pin #	Name	I/O	Type	Description
34	P10	I/O	Digital	• GPIO10: general-purpose I/O • DL_UART_RX: UART flash download receive data input • UART0_RX: receive data input • SDIO_DATA2: data • CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M)
35	P11	I/O	Digital	• GPIO11: general-purpose I/O • DL_UART_TX: UART flash download transmit data output • UART0_TX: transmit data output • SDIO_DATA3: data
36	P14	I/O	Digital	• GPIO14: general-purpose I/O • SDIO_CLK: clock • SPI0_SCK: serial clock • BT_ANT0: Bluetooth antenna select • I2C1_SCL: serial clock
37	P15	I/O	Digital	• GPIO15: general-purpose I/O • SDIO_CMD: command/response • SPI0_CSN: chip select • BT_ANT1: Bluetooth antenna select • I2C1_SDA: serial data
38	P16	I/O	Digital	• GPIO16: general-purpose I/O • SDIO_DATA0: data • SPI0_MOSI: master out slave in • BT_ANT2: Bluetooth antenna select
39	P17	I/O	Digital	• GPIO17: general-purpose I/O • SDIO_DATA1: data • SPI0_MISO: master in slave out • BT_ANT3: Bluetooth antenna select
40	P18	I/O	Digital	• GPIO18: general-purpose I/O • SDIO_DATA2: data • PWMG0_PWM0: PWM0 channel of PWMG0

Pin #	Name	I/O	Type	Description
41	P19	I/O	Digital	• GPIO19: general-purpose I/O • SDIO_DATA3: data • PWMG0_PWM1: PWM1 channel of PWMG0
42	P43	I/O	Digital	• GPIO43: general-purpose I/O • I2C1_SDA: serial data • I2S1_DOUT: serial data output • SC_VCC: power supply to the smart card
43	P42	I/O	Digital	• GPIO42: general-purpose I/O • I2C1_SCL: serial clock • I2S1_DIN: serial data input • LIN_SLEEP: transceiver sleep mode (active low) • SC_RSTN: reset
44	P41	I/O	Digital	• GPIO41: general-purpose I/O • UART2_TX: transmit data output • I2S1_SYNC: frame synchronization • LIN_TXD: transmit data output • SC_IO: data input/output
45	P40	I/O	Digital	• GPIO40: general-purpose I/O • UART2_RX: receive data input • I2S1_SCK: serial clock • LIN_RXD: receive data input • SC_CLK: clock
46	VCCIF	-	Analog input	IF power supply
47	VCCA	-	Analog input	Analog power supply
48	VDDPA_BT	-	Analog output	Bluetooth RF PA LDO output
49	VCCRXFE	-	Analog input	RF receiver power supply
50	GND	-	GND	Ground
51	ANT	-	RF	2.4 GHz RF signal port
52	VCCPA	-	Analog input	RF PA power supply
53	VCCPAD	-	Analog input	RF PA driver power supply
54	XO	-	Analog output	26 MHz crystal output

Pin #	Name	I/O	Type	Description
55	XI	-	Analog input	26 MHz crystal input
56	VCCPLL	-	Analog input	RF PLL power supply
Die pad	GND_SLUG	-	GND	Ground

3.2 Pin Multiplexing

Table 3-2 shows the pin mux functions of GPIOs.

Table 3-2 Pin Multiplexing

GPIO	Flash Download	Alternate Functions						
		AF1	AF2	AF3	AF4	AF5	AF6	AF7
	UART	UART1 SPI1 Clock UART0 SDIO I2C0 IrDA UART2 I2C1	I2C1 SDIO PWMG0 SPI0 SWD Clock I2S1	SWD Clock AoA/AoD AUX ADC LIN	Smart Card I2C1 QSPI0	AUX ADC LIN	LIN	QSPI1
GPIO0		UART1_TX	I2C1_SCL	SWCLK	SC_IO	ADC12	LIN_TXD	
GPIO1		UART1_RX	I2C1_SDA	SWDIO	SC_CLK	ADC13	LIN_RXD	
GPIO2		SPI1_SCK	SDIO_CLK		SC_RSTN	LIN_SLEEP		QSPI1_SCK
GPIO3		SPI1_CSN	SDIO_CMD		SC_VCC			QSPI1_CS
GPIO4		SPI1_MOSI	SDIO_DATA0					QSPI1_IO0
GPIO5		SPI1_MISO	SDIO_DATA1					QSPI1_IO1
GPIO6		CLK13M	PWMG0_PWM0					QSPI1_IO2

GPIO	Flash Download	Alternate Functions						
		AF1	AF2	AF3	AF4	AF5	AF6	AF7
	UART	UART1 SPI1 Clock UART0 SDIO I2C0 IrDA UART2 I2C1	I2C1 SDIO PWMG0 SPI0 SWD Clock I2S1	SWD Clock AoA/AoD AUX ADC LIN	Smart Card I2C1 QSPI0	AUX ADC LIN	LIN	QSPI1
GPIO7			PWMG0_PWM1					QSPI1_IO3
GPIO10	DL_UART_RX	UART0_RX	SDIO_DATA2	CLK_AUXS_CIS				
GPIO11	DL_UART_TX	UART0_TX	SDIO_DATA3					
GPIO14		SDIO_CLK	SPI0_SCK	BT_ANT0	I2C1_SCL			
GPIO15		SDIO_CMD	SPI0_CSN	BT_ANT1	I2C1_SDA			
GPIO16		SDIO_DATA0	SPI0_MOSI	BT_ANT2				
GPIO17		SDIO_DATA1	SPI0_MISO	BT_ANT3				
GPIO18		SDIO_DATA2	PWMG0_PWM0					
GPIO19		SDIO_DATA3	PWMG0_PWM1					
GPIO20		I2C0_SCL	SWCLK					
GPIO21		I2C0_SDA	SWDIO	ADC6				

GPIO	Flash Download	Alternate Functions						
		AF1	AF2	AF3	AF4	AF5	AF6	AF7
	UART	UART1 SPI1 Clock UART0 SDIO I2C0 IrDA UART2 I2C1	I2C1 SDIO PWMG0 SPI0 SWD Clock I2S1	SWD Clock AoA/AoD AUX ADC LIN	Smart Card I2C1 QSPI0	AUX ADC LIN	LIN	QSPI1
GPIO22		CLK26M	PWMG0_PWM2	ADC5	QSPI0_SCK			
GPIO23			PWMG0_PWM3	ADC3	QSPI0_CS			
GPIO24		LPO_CLK	PWMG0_PWM4	ADC2	QSPI0_IO0			
GPIO25		IRDA	PWMG0_PWM5	ADC1	QSPI0_IO1			
GPIO26					QSPI0_IO2			
GPIO27		CIS_MCLK	CLK_AUXS_CIS		QSPI0_IO3			
GPIO40		UART2_RX	I2S1_SCK	LIN_RXD	SC_CLK			
GPIO41		UART2_TX	I2S1_SYNC	LIN_TXD	SC_IO			
GPIO42		I2C1_SCL	I2S1_DIN	LIN_SLEEP	SC_RSTN			
GPIO43		I2C1_SDA	I2S1_DOUT		SC_VCC			

4. Functional Description

4.1 Wi-Fi/Bluetooth Transceiver

The BK7257 integrates a high-performance Wi-Fi/Bluetooth transceiver. The transceiver incorporates two on-chip baluns. On the receive side, the on-chip balun converts the single-ended (unbalanced) RF signal from the antenna into a differential (balanced) signal and the low noise amplifier (LNA) amplifies the differential signal to achieve a better noise and linearity trade-off. On the transmit side, the power amplifier (PA) amplifies the differential signal and the on-chip balun converts the differential signal to a single-ended signal for feeding the antenna. This enables transmit and receive operations with only one ANT pin connected to the antenna. The frequency synthesizer is fully integrated, eliminating the need for any external components.

4.2 Clock Management

The primary clock sources available in the BK7257 are as follows:

- High-frequency clocks
  - 26 MHz crystal oscillator: it outputs clock signal XTALH
  - 26–360 MHz internal digitally controlled oscillator (DCO): it outputs clock signal CLK_DCO
  - Digital PLL (DPLL): it generates 320 MHz clock CLK_320M and 480 MHz clock CLK_480M
- Low-frequency clock
  - 32 kHz internal ring oscillator (ROSC): it outputs clock signal CLK_ROSC
- Audio clock
  - Audio PLL (APLL): its default frequency is 98.304 MHz, and it outputs clock signal CLK_APLL

The system generates a low-power clock source LPO_CLK for standby. The LPO_CLK can be selected from the following clocks:

- 32 kHz clock signal derived from 26 MHz crystal oscillator
- 32 kHz internal oscillator ROSC

The BK7257 also has a clock output capability, which allows clock signals to be output to external components through GPIOs. GPIOs can output the following clock signals:

- CLK13M: clock derived from CLK_XTAL (division factor 1/2/4/8)
- CLK26M: high-frequency crystal clock CLK_XTAL, generally 26 MHz
- LPO_CLK: LPO_CLK clock

- CLK_AUXS_CIS: reference clock for external CMOS image sensor (CIS)
- CIS_MCLK: reference clock for external CMOS image sensor (CIS)

4.3 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, and wake-up from shutdown mode or deep sleep mode.

Power-on reset, brown-out reset, and AWDT watchdog reset reset the whole chip to its initial state. The DWDT watchdog reset's reset scope is configurable and can be configured to reset the whole chip.

Wake-up from shutdown mode triggers the whole system reset, while wake-up from deep sleep mode triggers the reset of digital blocks.

4.4 Power Management

4.4.1 Power Scheme

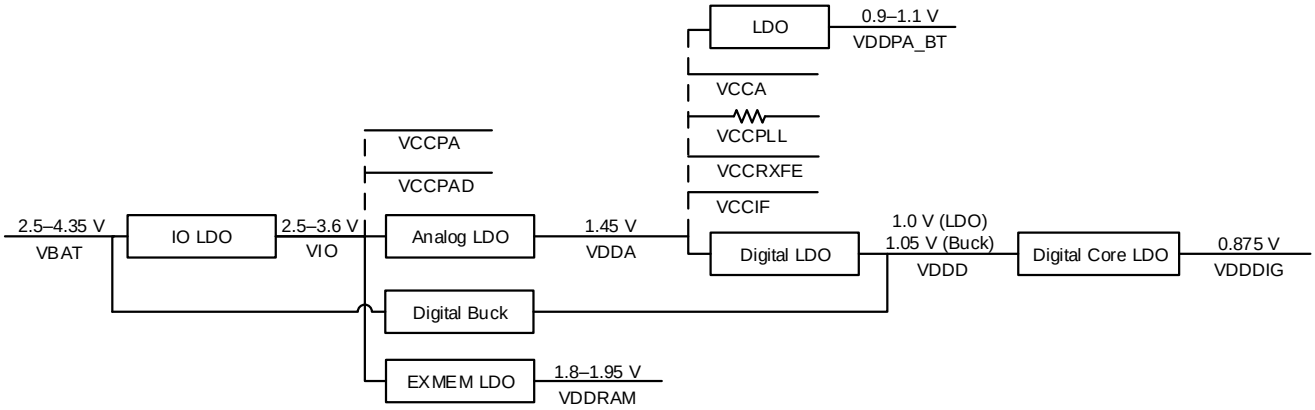
The power management system on the BK7257 includes a buck converter and several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

The VBAT is the external main chip supply ranging from 2.5 to 4.35 V. The VBAT generates VIO through the IO LDO regulator. In addition to being the power supply for the Wi-Fi PA, the VIO is also the input supply of analog LDO, digital buck, and EXMEM LDO. The VBAT also generates VDDD through the digital buck converter. The LDOs and buck generate the following main power supplies:

- VDDA: power supply for RF/analog blocks. It is externally connected to VCCA, VCCPLL, VCCRXFE, and VCCIF to supply power to the Wi-Fi/Bluetooth transceiver, and internally provides power to XTAL and AUDIO directly.
- VDDDIG: power supply for digital domain. It provides power supply for the processor, memories, Wi-Fi and Bluetooth basebands, as well as various peripherals.

Figure 4-1 shows the power distribution of the BK7257.

Figure 4-1 Internal Power Distribution



Note: Outputs from the buck converter and LDO regulators require proper bypass capacitors to reduce supply noise. Please refer to the hardware schematic for details on selecting bypass capacitors.

Figure 4-2 shows the power-up sequence of the BK7257.

Figure 4-2 BK7257 Power-up Sequence

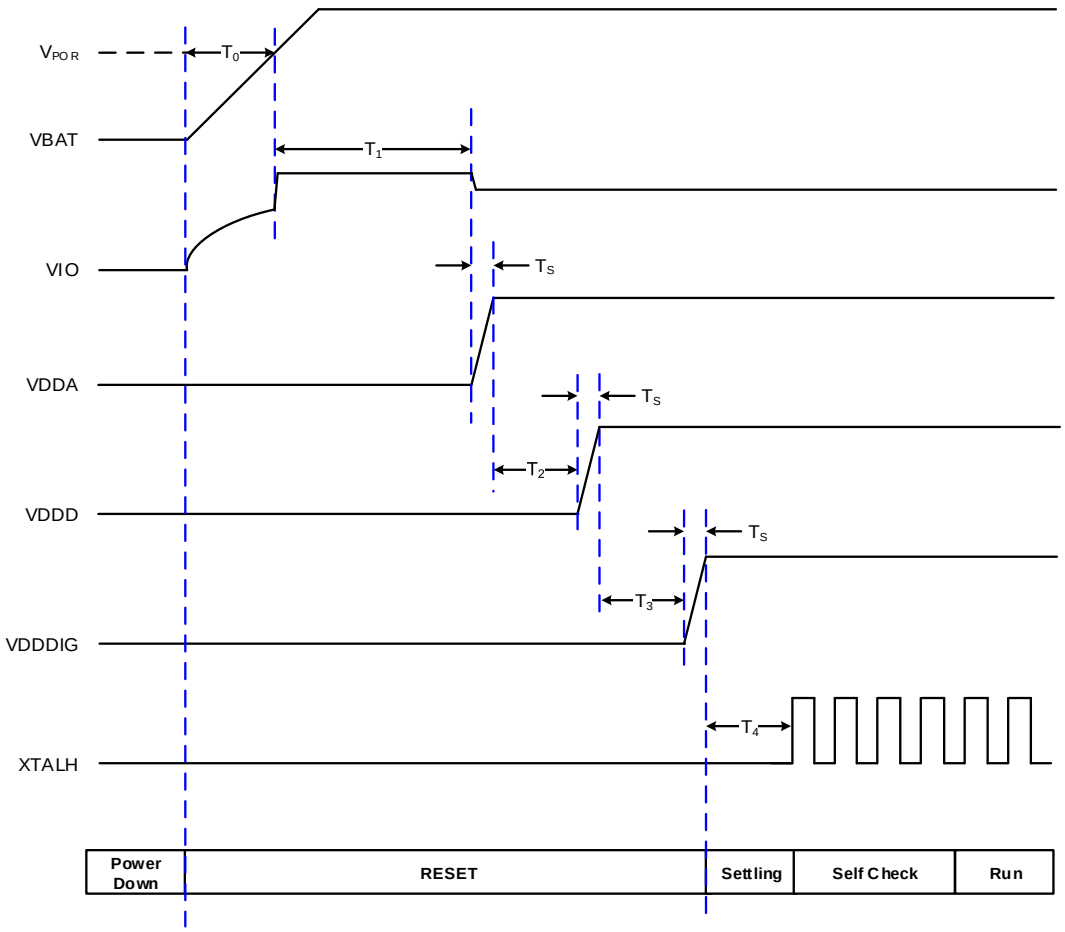


Table 4-1 Timing Parameters of Power-up Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
V_{POR}	VBAT POR threshold	-	1.95	-	V
T_0	IO LDO settle time	200	-	-	µs
T_1(1)	IO LDO ready time	-	-	500	µs
T_2	Analog LDO ready time	-	240	500	µs
T_3	Digital buck/LDO ready time	-	240	500	µs
T_4	Digital core LDO ready time/XTALH stable time	100	-	-	µs
T_S	LDO (excl. IO LDO) settle time	0	-	-	µs

(1) If the VBAT slew rate is greater than 3.3 kV/s, VIO will overshoot.

Figure 4-3 shows the power-down sequence of the BK7257.

Figure 4-3 BK7257 Power-down Sequence

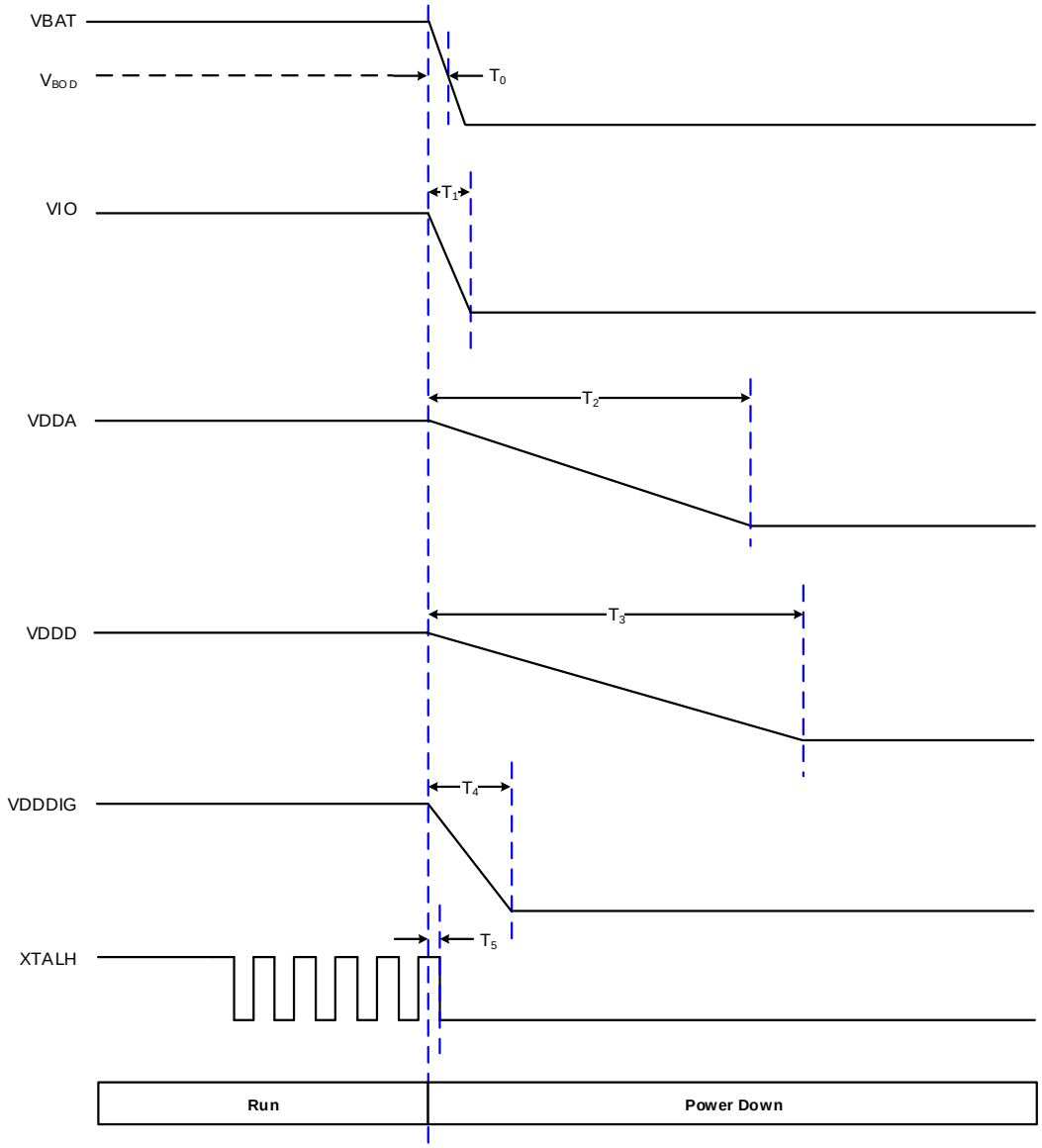


Table 4-2 Timing Parameters of Power-down Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
V_{BOD}	VBAT BOD threshold	-	1.85	-	V
T_0	VBAT power-down time	-	400	-	μs
T_1	IO LDO power-down time	-	600	-	μs
T_2	Analog LDO power-down time	-	400	-	ms

Parameter	Description	Min.	Typ.	Max.	Unit
T_3	Digital buck/LDO power-down time	-	500	-	ms
T_4	Digital core LDO power-down time	-	3.5	-	ms
T_5	XTALH power-down time	-	100	-	µs

4.4.2 Power Modes

The BK7257 supports three low-power modes except active mode, namely shutdown mode, deep sleep mode, and sleep mode, among which the shutdown mode has the lowest power consumption.

Shutdown Mode: All circuits are turned off. A high level on the CEN pin will bring the system to active mode.

Deep Sleep Mode: All circuits are powered down except the AON block. A GPIO event or an RTC event can power up the system again. The retention register holds its content.

Sleep Mode: The MCU and all digital blocks stop their clocks. A GPIO event, an RTC event, a Wi-Fi MAC counter event, or a Bluetooth MAC counter event can bring the system back to active mode with normal voltage.

Active Mode: The MCU is active, and all peripherals are available.

4.5 General-purpose I/Os (GPIO)

The BK7257 has up to 28 GPIOs, which can be configured as either input or output. All GPIOs are shared with alternate functions. Table 3-2 Pin Multiplexing provides the mux functions of GPIOs.

The main features of GPIOs include:

- Push-pull
- Internal pull-up/down resistors
- Configurable drive strength
- Alternate function
- Interrupt generation:
  - High or low level
  - Rising or falling edge

4.6 SPI Interfaces (SPI)

The BK7257 integrates two SPI interfaces that can operate in master or slave mode. The SPI interfaces allow a clock frequency up to 40 MHz in both master and slave modes.

The SPI interfaces support the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Configurable 8-bit or 16-bit data width
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Embedded 64-depth RX FIFO and 64-depth TX FIFO with DMA capability

4.7 Quad SPI Interfaces (QSPI)

The BK7257 embeds two Quad SPI interfaces that provide support for communicating with external flash, PSRAM, or AMOLED display. The QSPI interfaces allow communicating up to 80 MHz.

The features of the QSPI interfaces are listed below:

- Single, dual, or quad SPI input/output
- Two functional modes: indirect mode and memory-mapped mode
- Fully programmable opcode and frame format
- Integrated RX FIFO and TX FIFO
- Supports 8, 16, and 32-bit data accesses

4.8 UART Interfaces (UART)

The BK7257 includes three Universal Asynchronous Receiver/Transmitter (UART) interfaces, which support full-duplex, asynchronous serial communication at a baud rate up to 6 Mbps.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bits)
- Even, odd, or none parity check
- Programmable stop bits (1 or 2 bits)
- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.
- Flash download (UART0)
- Programmable digital filter

4.9 Smart Card Controller (SC)

The Smart Card controller (SC) is a communication controller that transmits data between the superior system and the Smart Card. The controller can perform a complete smart card session, including card activation, card deactivation, cold/warm reset, Answer to Reset (ATR) response reception, data transfers, etc.

The features of the Smart Card controller (SC) are listed below:

- Supports the ISO/IEC 7816-3:2006 and EMV 4.3 specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Extensive interrupt support system
- Adjustable clock rate and bit (baud) rate
- Configurable automatic byte repetition
- Handles commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission, and
  - T=1 for asynchronous half-duplex block transmission
- Automatic convention detection
- Adjustable FIFOs for Receive and Transmit buffers (64 bytes) with threshold
- Configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers

4.10 SDIO Interface (SDIO)

A secure digital input/output (SDIO) host/slave interface is available on the BK7257. It can be used as a host to read external SD cards or used by an external host as a slave to communicate with chips. The SDIO interface allows a maximum clock speed of 80 MHz.

The SDIO features include the following:

- SD memory card specification version 2.0 compliant

- SDIO card specification version 2.0 compliant
- Two data bus modes: 1-bit mode (default) and 4-bit mode
- Data transfer up to 40 Mbyte/s for the host mode and 20 Mbyte/s for the slave mode
- Supports DMA capability, allowing high-speed transfer without CPU load

4.11 I2C Interfaces (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7257 embeds two I2C interfaces, which can operate in master or slave mode.

The features of the I2C interfaces are listed below:

- Master and slave modes
- Standard mode (up to 100 kbps)
- Fast mode (up to 400 kbps)
- 7-bit and 10-bit addressing
- Bus idle and SCL low timeout condition detection
- Embedded 16-byte TX FIFO and 16-byte RX FIFO

4.12 USB Controller (USB)

The BK7257 embeds a USB high-speed (up to 480 Mbps) controller with an integrated transceiver. It can operate as a host or a device.

The USB controller features are the following:

- Compliant with the Universal Serial Bus Specification Rev 1.1 and 2.0
- Full-speed (FS) operation (up to 12 Mbps) and high-speed operation (up to 480 Mbps)
- One bidirectional control endpoint0
- Seven IN/OUT endpoints configurable to support bulk, interrupt or isochronous data transfer
- A FIFO of 8 Kbytes configurable to be allocated to 8 endpoints
- USB 2.0 Link Power Management (LPM) support

4.13 LIN Controller (LIN)

The Local Interconnect Network (LIN) controller is a communication controller that performs serial communication. It implements the data link layer of the LIN Protocol Specification. The LIN protocol uses a single master/multiple slave concept for the frame transfer between nodes of the LIN network.

The LIN controller supports Sleep mode. If a low level is applied to the LIN_SLEEP pin, the external transceiver enters the Sleep mode.

The features of the LIN controller are listed here:

- Support of LIN specification 2.2A
- Backward compatibility to LIN 1.3
- Configurable for support of master or slave functionality
- Programmable data rate between 1 kbit/s and 20 kbit/s (for master)
- Automatic bit rate detection (for slave)
- 8-byte data buffer
- 8-bit host controller interface

4.14 GDMA Controllers (GDMA)

The BK7257 has two general-purpose DMA controllers (GDMA) with 8 DMA channels each to unload CPU activity. The 8 channels are shared by peripherals that have DMA capabilities.

The GDMA controllers can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word), or 32 bits (word). The GDMA controllers allow peripheral to memory, memory to memory, and memory to peripheral data transfers at a high speed.

The GDMA controllers support channel isolation. The DMA channels can be configured as secure/non-secure and as privileged/unprivileged channels:

- A non-secure channel performs non-secure DMA transfers
- A secure channel can perform secure or non-secure DMA transfers, with
  - Secure or non-secure data read from the source address
  - Secure or non-secure data write to the destination address
  - Via a TrustZone-aware DMA AHB master port
- An unprivileged channel performs unprivileged DMA transfers
- A privileged channel performs privileged DMA transfers

A selection of peripherals on the BK7257 have DMA capabilities, including UART0, UART1, UART2, SPI0, SPI1, SDIO, AUDIO, I2S1, JPEG encoder, AUX ADC, and H.264.

4.15 DMA2D Controller (DMA2D)

The BK7257 has a specialized DMA controller (DMA2D) dedicated to image processing, offering direct memory transfer and 2D graphical acceleration without CPU intervention. It can perform the following operations:

- Filling a part or the whole of a destination image with a fixed color
- Copying a part or the whole of a source image into a part or the whole of a destination image
- Copying a part or the whole of a source image into a part or the whole of a destination image with a pixel format conversion
- Blending a part or two complete source images with a different pixel format and copying the result into a part or the whole of a destination image with a different color format

The DMA2D controller supports six operating modes:

- Register to memory
- Memory to memory
- Memory to memory with pixel format conversion
- Memory to memory with pixel format conversion and blending
- Memory to memory with pixel format conversion, blending and fixed color foreground layer
- Memory to memory with pixel format conversion, blending and fixed color background layer

Up to 12 input color modes are supported from 4-bit up to 32-bit per pixel with indexed or direct color coding. Six output color modes including RGB, ARGB, and YUV are supported. The DMA2D features dedicated memories for color lookup table (CLUT) storage.

An interrupt can be generated on the following events:

- Configuration error
- CLUT transfer completion
- CLUT access error
- Watermark on a user programmable destination line
- Transfer completion
- Transfer error

4.16 Rotation Module (ROTT)

The rotation module (ROTT) is capable of performing the following operations:

- Convert a YUV422 image stored in memory to a RGB565 image.
- Rotate a YUV422 or RGB565 image by 90° in either clockwise or counterclockwise direction.
- Store the converted or rotated image into the target memory.

4.17 Scaling Modules (SCALE)

The BK7257 has two scaling modules (SCALE) that can scale images of Y0UY1V, RGB565, or RGB888 format without changing the data format.

4.18 JPEG Encoder/Decoder

The BK7257 includes a JPEG encoder and a JPEG decoder for encoding and decoding JPEG streams. The JPEG encoder provides a small hardware compressor for JPEG images, while the decoder provides a decompression accelerator for JPEG images. Additionally, the JPEG encoder supports up to 32 programmable quantization tables.

4.19 H.264 Encoder (H.264)

The H.264 video encoder allows fast and simple video compression. It performs the H.264 video compression algorithm on an incoming video stream. The encoded bitstream can be decoded by a Baseline, Mainprofile decoder. The input is raster 4:2:0 YUV video data. This data is compressed into H.264-compliant byte stream NAL units.

The H.264 supports the following features:

- Fully compatible with the ITU-T H.264 specification
- Level 1 to 4.1, encoded stream can be decoded by Baseline, Main profile decoder
- Supports up to 720p (1280x720 @ 30 fps)
- Constant Bit Rate and partial Variable Bit Rate mode support
- Motion vector up to –16.00/+15.75 pixels (search area is 32x32 pixels wide down to quarter pixel)
- Support for all intra16x16 and all but two of intra4x4 prediction modes
- Block skipping logic for lower bitrate
- Supports picture cropping for image sizes that are not a multiple of 16 pixels
- Supports Chroma Quantization Parameter offset for increased compression

- Requires no external memory by using Compressed framestore (CFS) for reference frame storage

4.20 PWM Group (PWMG)

The BK7257 has an advanced-control PWM group (PWMG). The PWMG consists of four independent 32-bit auto-reload counters driven by four programmable prescalers. The PWMG can generate pulse width modulated signals for a variety of purposes, including input capture, pulse edge counting, or generation of output waveforms (output compare).

The features of the PWMG are listed here:

- Four 32-bit up, down, or up-and-down auto-reload counters:
  - PWM0 has a counter.
  - PWM1 has a counter (up-counting mode only).
  - PWM2 and PWM3 share a counter.
  - PWM4 and PWM5 share a counter.
- Four 8-bit programmable prescalers capable of dividing the clock frequency of each counter by any factor between 1 and 256
- Four independent channels, among which:
  - PWM0/2/4
    - Input capture
    - Pulse edge counting
    - PWM generation (edge or center-aligned mode)
  - PWM1
    - Independent simple waveform generation (up-counting mode)
    - Coupled waveform (reverse or identical) generation when coupled with PWM0
- Two channels PWM3/5 capable of generating coupled waveforms (reverse or identical) when coupled with PWM2/4 respectively
- Complementary outputs with programmable dead-time and configurable dead-time mode
- Synchronization circuit to control the counter with external signals and to interconnect several counters together
- Repetition counter to update the registers only after a given number of cycles of the counter
- Interrupt generation on the following events:
  - Update: counter overflow or underflow, counter initialization (by software or internal/external trigger)
  - Counter start
  - Input capture
  - Output compare

- Change of polarity, duty cycle, and base frequency on every PWM period
- Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes

Table 4-3 below provides the description of PWM signals.

Table 4-3 PWM Signals

GPIO	PWM Pin Name	Signal Type	Description
GPIO6/GPIO18	PWMG0_PWM0	I/O	PWM0 channel of PWMG0
GPIO7/GPIO19	PWMG0_PWM1	I/O	PWM1 channel of PWMG0 PWM1 can work independently to generate simple waveforms or couple with PWM0 (with deadtime insertion) to generate reverse or identical waveforms of PWM0.
GPIO22(1)	PWMG0_PWM2	I/O	PWM2(2) channel of PWMG0
GPIO23(1)	PWMG0_PWM3	I/O	PWM3(2) channel of PWMG0 PWM3 can couple with PWM2 (with deadtime insertion) to generate reverse or identical waveforms of PWM2.
GPIO24	PWMG0_PWM4	I/O	PWM4(3) channel of PWMG0
GPIO25	PWMG0_PWM5	I/O	PWM5(3) channel of PWMG0 PWM5 can couple with PWM4 (with deadtime insertion) to generate reverse or identical waveforms of PWM4.

(1) It is not recommended to use GPIO22 and GPIO23 for LED and motor control.
(2) When PWM2 and PWM3 are enabled simultaneously, they cannot generate waveforms with different duty cycles.
(3) When PWM4 and PWM5 are enabled simultaneously, they cannot generate waveforms with different duty cycles.

4.21 I2S Interface (I2S)

The BK7257 integrates an I2S interface that supports master and slave modes with sampling rates from 8 kHz to 384 kHz.

The I2S interface supports both PCM mono channel mode and I2S stereo channel mode.

Listed here are the I2S features:

- Master or slave mode
- Full duplex or half-duplex communication
- Various sampling rates
- 12-bit programmable prescaler
- Multiple I2S protocols supported:
  - I2S Philips standard

  - MSB-Justified standard (Left-Justified)
  - LSB-Justified standard (Right-Justified)
  - PCM standard
- Programmable data order with LSB first or MSB first
- Programmable data width between 1 and 32 bits
- Programmable clock polarity
- Integrated 32-bit RX FIFO and 32-bit TX FIFO, both with a depth of 32 x 3 channels

4.22 Audio Peripherals

The BK7257 comes with a rich set of audio peripherals to enhance the listening experience. The chip includes a four-band digital equalizer, two analog-to-digital converters (ADC), a digital-to-analog converter (DAC), two microphone input amplifiers and a bias generator, an audio amplifier, an SBC decoder accelerator, etc.

4.22.1 Four-band Digital Equalizer (EQ)

A dedicated four-band digital equalizer is implemented prior to digital-to-analog conversion, allowing the user to customize the frequency response of the audio output. The equalizer is implemented in hardware to reduce overall chip power consumption.

4.22.2 Audio ADCs and DAC

The BK7257 contains two 16-bit ADCs with sampling rates of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz. The chip also integrates a 16-bit DAC with sampling rates of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz.

4.22.3 Microphone Input Amplifiers and Bias Generator

The BK7257 contains two fully differential analog microphone input amplifiers and a low-noise microphone bias generator, allowing the microphone to interface with passive resistors and capacitors.

The microphone signal can be amplified with the amplifier over a 0 to 32 dB gain range with a 2 dB step size.

4.22.4 Audio Amplifier

The BK7257 provides a high-quality audio amplifier capable of driving a 16 Ω speaker with load capacitance up to 30 pF.

4.23 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 12-bit successive approximation analog-to-digital converter. The AUX ADC has multiple external analog input channels and internal dedicated channels. The AUX ADC supports A/D conversion performed in one-shot, software control, or continuous mode.

The AUX ADC module has the following features:

- Programmable sampling rate from 12.5 to 812.5 kHz
- 12-bit resolution
- Up to 7 external analog input channels: ADC1/2/3/5/6/12/13
- Five internal dedicated channels:
  - VBAT monitoring channel (VBAT/2, VBAT/3, VBAT/5, or VBAT/7), connected to ADC0
  - Internal temperature sensor (TEMP), connected to ADC7
  - TSSIO, connected to ADC8
  - Two internal debug channels, connected to ADC9/11
- Conversion modes:
  - One-shot mode
  - Software control mode
  - Continuous mode

4.24 Timer Groups (TIMG)

The BK7257 includes two general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, division factor between 1 and 16
- Capable of reading the real-time value of the counter

4.25 Watchdog Timers (WDT)

The BK7257 has two watchdog timers, the digital power domain watchdog timer (DWDT) and the AON power domain watchdog timer (AWDT). The purpose of the watchdog timers is to detect and recover from failures or malfunctions. The watchdog timers trigger a reset on expiry of a specified time period.

The DWDT runs on the 32 kHz LPO_CLK clock (division factor 2/4/8/16) and has a maximum programmable period of up to 32.768 (2^16/2 kHz) seconds. The AWDT runs on the ROSC and has a maximum programmable period of up to 65.536 (2^16/1 kHz) seconds.

4.26 Real-time Counter (RTC)

The real-time counter (RTC) module features a 64-bit counter and a tick event generator. The RTC runs on the 32 kHz LPO_CLK clock. It is used for low-power timing, and it can keep running even when the system is in deep sleep mode.

4.27 IrDA Interface (IRDA)

The BK7257 embeds a hardware IrDA interface that supports waveform analysis and waveform generation. It monitors the start of infrared signals, records the sequence of infrared waveforms, stores the waveforms in the RX FIFO for software analysis, and writes the waveforms to be sent to the TX FIFO when sending, thereby enabling the analysis and transmission of any infrared protocol.

The IrDA has the following features:

- Single-duplex mode
- Carrier modulation for transmission
- Integrated 512-byte RX FIFO and 512-byte TX FIFO

4.28 Temperature Sensor

The BK7257 integrates an on-chip temperature sensor that can measure on-chip temperature over -40 to +125 °C with an accuracy of ±5 °C. The digital results can be read from the AUX ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
VBAT	Chip power supply voltage	-0.3	4.35	V
VIO	IO LDO output voltage	-0.3	4.0	V
VCCPA	Supply voltage for PA	-0.3	4.0	V
VCCPAD	Supply voltage for PA driver	-0.3	4.0	V
VCCIF	Supply voltage for IF	-0.3	1.8	V
VCCRXFE	Supply voltage for RX	-0.3	1.8	V
VCCPLL	Supply voltage for RF PLL	-0.3	1.8	V
VCCA	Supply voltage for analog	-0.3	1.8	V
VDDPA_BT	Bluetooth RF PA LDO output voltage	-0.3	1.2	V
VDDA	Analog LDO output voltage	-0.3	1.8	V
VDDD	Digital LDO output voltage	-0.3	1.2	V
	Digital buck output voltage	-0.3	1.2	V
VDDDIG	Digital core LDO output voltage	-0.3	1.1	V
VDDRAM	EXMEM LDO output voltage	-0.3	2.1	V
SWD	Digital buck switch output voltage	-0.3	4.35	V
MICBIAS	Microphone bias output voltage	-0.3	4.0	V
P_{RX}	RX input power	-	10	dBm
T_{STR}	Storage temperature range	-55	150	℃

5.2 ESD Ratings

Parameter	Description	Test Condition	Value	Unit
ESD HBM	Electrostatic discharge voltage (human body model), per ANSI/ESDA/JEDEC JS-001	-	±3000	V
ESD CDM	Electrostatic discharge voltage (charge device model), per ANSI/ESDA/JEDEC JS-002	-	±500	V

5.3 Recommended Operating Conditions

Parameter	Description	Min.(1)	Typ.	Max.	Unit
VBAT(2)	Chip power supply voltage	2.5	3.3	4.35	V
VBAT slew rate	-	300	-	-	mV/ms
VIO	IO LDO output voltage	2.5	-	3.6	V
VCCPA(2)	Supply voltage for PA	2.5	-	3.6	V
VCCPAD(2)	Supply voltage for PA driver	2.5	-	3.6	V
VCCIF	Supply voltage for IF	-	1.45	-	V
VCCRXFE	Supply voltage for RX	-	1.45	-	V
VCCPLL	Supply voltage for RF PLL	-	1.45	-	V
VCCA	Supply voltage for analog	-	1.45	-	V
VDDPA_BT	Bluetooth RF PA LDO output voltage	0.9	-	1.1	V
VDDA	Analog LDO output voltage	-	1.45	-	V
VDDD	Digital LDO output voltage	-	1.0	-	V
	Digital buck output voltage	-	1.05	-	V
VDDDIG	Digital core LDO output voltage	-	0.875	-	V
VDDRAM	EXMEM LDO output voltage	1.8	-	1.95	V
MICBIAS	Microphone bias output voltage	1.8	-	2.4	V
T_{OPR}	Operating temperature range	-40	-	85	℃

(1) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. Care must be taken when operating at the minimum specified voltage.

(2) To ensure WLAN performance, the ripple on the supply must be less than Vpp = 100 mV.

5.4 Digital I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIH	High-level input voltage	-	0.7 VIO	-	VIO + 0.3	V
VIL	Low-level input voltage	-	-0.3	-	0.3 VIO	V
VOH	High-level output voltage	-	0.8 VIO	-	-	V
VOL	Low-level output voltage	-	-	-	0.1 VIO	V
I_{DRV}	I/O output drive strength	-	5	-	20	mA
R_{PU}	Weak pull-up resistor	-	-	40	-	kΩ
R_{PD}	Weak pull-down resistor	-	-	44	-	kΩ

5.5 IO LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VIO	IO LDO output voltage	2.5	3.3	3.6	V
Load current	-	-	-	500	mA

5.6 Analog LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDA	Analog LDO output voltage	-	1.45	-	V
Load current	-	-	-	150	mA

5.7 Digital LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDD	Digital LDO output voltage	-	1.0	-	V
Load current	-	-	-	100	mA

5.8 Core LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDDIG	Digital core LDO output voltage	-	0.875	-	V
Load current	-	-	-	100	mA

5.9 Digital Buck

Parameter	Description	Min.	Typ.	Max.	Unit
VDDD	Digital buck output voltage	-	1.05	-	V
Load current	-	-	-	100	mA
Switching frequency	Buck modulation frequency	0.5	1	2	MHz
Output filter capacitor capacitance	-	-	4.7	-	μF
Inductor inductance	-	-	4.7	-	μH
Inductor DC resistance	-	-	-	500	mΩ
Inductor saturation current	-	200	-	-	mA

5.10 26 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F0	Nominal frequency	-	-	26	-	MHz
ΔF/F0	Frequency tolerance	25 ℃	-10	-	+10	ppm
TC	Frequency stability over operating temperature	-40 to 105 ℃ crystal	-20	-	+20	ppm
		-30 to 85 ℃ crystal	-10	-	+10	ppm
CL	Load capacitance	-	7	7.3	12	pF
TS	Trim sensitivity	-40 to 105 ℃ crystal	-	32	-	ppm/pF
		-30 to 85 ℃ crystal	-	17	-	ppm/pF

5.11 Current Consumption

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
Active Mode					
RX current	11b: 11 Mbps DSSS	-	17.5	-	mA
	11g: 54 Mbps OFDM	-	17.5	-	mA
	11n: MCS7, HT20	-	17.5	-	mA
	11n: MCS7, HT40	-	18.5	-	mA
	11ax: MCS7, HE20	-	17.5	-	mA
TX current	11b: 11 Mbps DSSS @ 19 dBm	-	235	-	mA
	11g: 54 Mbps OFDM @ 17 dBm	-	200	-	mA
	11n: MCS7, HT20 @ 16 dBm	-	189	-	mA
	11n: MCS7, HT40 @15 dBm	-	182	-	mA
	11ax: MCS7, HE20 @ 16 dBm	-	188	-	mA
Sleep Mode					
Sleep	-	-	43	-	µA
Deep sleep	-	-	16	-	µA
Shutdown Mode					
Shutdown	-	-	2.5	-	µA

5.12 WLAN RF Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
Sensitivity					
Sensitivity - IEEE 802.11b	1 Mbps DSSS	-	-98	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
(8% PER for 1024 octet PSDU)	2 Mbps DSSS	-	-94.5	-	dBm
	5.5 Mbps DSSS	-	-92	-	dBm
	11 Mbps DSSS	-	-89	-	dBm
Sensitivity - IEEE 802.11g (10% PER for 1000 octet PSDU)	6 Mbps OFDM	-	-92	-	dBm
	9 Mbps OFDM	-	-91.5	-	dBm
	12 Mbps OFDM	-	-90.5	-	dBm
	18 Mbps OFDM	-	-88	-	dBm
	24 Mbps OFDM	-	-85	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-77.5	-	dBm
	54 Mbps OFDM	-	-76.5	-	dBm
Sensitivity - IEEE 802.11n, 20 MHz (10% PER for 4096 octet PSDU, LDPC)	HT20, MCS0	-	-92	-	dBm
	HT20, MCS1	-	-91	-	dBm
	HT20, MCS2	-	-88	-	dBm
	HT20, MCS3	-	-86	-	dBm
	HT20, MCS4	-	-82	-	dBm
	HT20, MCS5	-	-78	-	dBm
	HT20, MCS6	-	-76.5	-	dBm
	HT20, MCS7	-	-75	-	dBm
Sensitivity - IEEE 802.11n, 40 MHz (10% PER for 4096 octet PSDU, LDPC)	HT40, MCS0	-	-87.5	-	dBm
	HT40, MCS1	-	-87	-	dBm
	HT40, MCS2	-	-85	-	dBm
	HT40, MCS3	-	-82.5	-	dBm
	HT40, MCS4	-	-79	-	dBm
	HT40, MCS5	-	-75	-	dBm
	HT40, MCS6	-	-74	-	dBm
	HT40, MCS7	-	-71.5	-	dBm
Sensitivity - IEEE 802.11ax, 20 MHz	HE20, MCS0	-	-92	-	dBm

Parameter	Condition		Min.	Typ.	Max.	Unit
(10% PER for 4096 octet PSDU, LDPC)	HE20, MCS1		-	-90.5	-	dBm
	HE20, MCS2		-	-87.5	-	dBm
	HE20, MCS3		-	-85	-	dBm
	HE20, MCS4		-	-81	-	dBm
	HE20, MCS5		-	-77.5	-	dBm
	HE20, MCS6		-	-75.5	-	dBm
	HE20, MCS7		-	-74	-	dBm
Sensitivity - IEEE 802.11ax, 40 MHz (10% PER for 4096 octet PSDU, LDPC)	HE40, MCS0		-	-88.5	-	dBm
	HE40, MCS1		-	-87.5	-	dBm
	HE40, MCS2		-	-85.5	-	dBm
	HE40, MCS3		-	-82	-	dBm
	HE40, MCS4		-	-77	-	dBm
	HE40, MCS5		-	-75	-	dBm
	HE40, MCS6		-	-74	-	dBm
	HE40, MCS7		-	-72	-	dBm
Maximum Receive Level						
Maximum receive level @ 2.4 GHz	11b: 1, 2 Mbps (8% PER, 1024 octets)		-	10	-	dBm
	11b: 5.5, 11 Mbps (8% PER, 1024 octets)		-	10	-	dBm
	11g: 6–54 Mbps (10% PER, 1000 octets)		-	0	-	dBm
	11n: MCS0–7 (10% PER, 4096 octets)		-	0	-	dBm
	11ax: MCS0–7 (10% PER, 4096 octets)		-	0	-	dBm
Adjacent Channel Rejection						
Adjacent channel (±30 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	1 Mbps DSSS	-74 dBm	-	50	-	dB
	2 Mbps DSSS	-74 dBm	-	45	-	dB

Parameter	Condition		Min.	Typ.	Max.	Unit
Adjacent channel (±25 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	5.5 Mbps DSSS	-70 dBm	-	43	-	dB
	11 Mbps DSSS	-70 dBm	-	40	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11g (10% PER for 1000 octet PSDU with desired signal level as specified in Condition)	6 Mbps OFDM	-79 dBm	-	43	-	dB
	54 Mbps OFDM	-62 dBm	-	27	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11n (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HT20, MCS0	-79 dBm	-	43	-	dB
	HT20, MCS7	-61 dBm	-	21	-	dB
Adjacent channel (±40 MHz) rejection - IEEE 802.11n (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HT40, MCS0	-76 dBm	-	TBD	-	dB
	HT40, MCS7	-58 dBm	-	TBD	-	dB
Adjacent channel (±20 MHz) rejection - IEEE 802.11ax (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HE20, MCS0	-79 dBm	-	43	-	dB
	HE20, MCS7	-61 dBm	-	26	-	dB
Adjacent channel (±40 MHz) rejection - IEEE 802.11ax (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HE40, MCS0	-76 dBm	-	TBD	-	dB
	HE40, MCS7	-58 dBm	-	TBD	-	dB
Spurious Emissions						
Spurious emissions	< 1 GHz		-	-60	-	dBm
	> 1 GHz		-	-50	-	dBm

5.13 WLAN RF Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
TX power					
TX power - IEEE 802.11b (SEM compliant)	1 Mbps DSSS	-	20	-	dBm
	11 Mbps DSSS	-	20	-	dBm
TX power - IEEE 802.11g (EVM compliant)	6 Mbps OFDM	-	18	-	dBm
	54 Mbps OFDM	-	18	-	dBm
TX power - IEEE 802.11n (EVM compliant)	HT20, MCS0	-	17	-	dBm
	HT20, MCS7	-	17	-	dBm
	HT40, MCS0	-	16	-	dBm
	HT40, MCS7	-	16	-	dBm
TX power - IEEE 802.11ax (EVM compliant)	HE20, MCS0	-	17	-	dBm
	HE20, MCS7	-	17	-	dBm
	HE40, MCS0	-	16	-	dBm
	HE40, MCS7	-	16	-	dBm
Spurious Emissions					
Spurious emissions (at maximum output power)	< 1 GHz	-	-50	-	dBm
	> 1 GHz	-	-45	-	dBm

5.14 Bluetooth LE RF Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz

Parameter	Condition	Min.	Typ.	Max.	Unit
Bluetooth LE 1 Mbps					
Sensitivity	30.8% PER	-	-97	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	8	-	dB
C/I 1 MHz adjacent channel	-	-	0	-	dB
C/I -1 MHz adjacent channel	-	-	0	-	dB
C/I 2 MHz adjacent channel	-	-	-26	-	dB
C/I -2 MHz adjacent channel	-	-	-27	-	dB
C/I 3 MHz adjacent channel	-	-	-28	-	dB
C/I -3 MHz adjacent channel	-	-	-29	-	dB
C/I > 3 MHz adjacent channel	-	-	-50	-	dB
C/I < -3 MHz adjacent channel	-	-	-50	-	dB
Out-of-band blocking	30–2000 MHz	-10	-	-	dBm
	2003–2399 MHz	-12	-	-	dBm
	2484–2997 MHz	-12	-	-	dBm
	3000 MHz–12.75 GHz	-2	-	-	dBm
Intermodulation	-	-	TBD	-	dBm
Bluetooth LE 2 Mbps					
Sensitivity	30.8% PER	-	-94	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	7	-	dB
C/I 2 MHz adjacent channel	-	-	0	-	dB
C/I -2 MHz adjacent channel	-	-	3	-	dB
C/I 4 MHz adjacent channel	-	-	-26	-	dB
C/I -4 MHz adjacent channel	-	-	-30	-	dB
C/I 6 MHz adjacent channel	-	-	-30	-	dB
C/I -6 MHz adjacent channel	-	-	-39	-	dB
C/I > 6 MHz adjacent channel	-	-	-22	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I < -6 MHz adjacent channel	-	-	-22	-	dB
Out-of-band blocking	30–2000 MHz	-	-30	-	dBm
	2003–2399 MHz	-	-35	-	dBm
	2484–2997 MHz	-	-35	-	dBm
	3000 MHz–12.75 GHz	-	-17	-	dBm
Intermodulation	-	-	TBD	-	dBm
Bluetooth LE 125 kbps					
Sensitivity	30.8% PER	-	-102	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	3	-	dB
C/I 1 MHz adjacent channel	-	-	-15	-	dB
C/I -1 MHz adjacent channel	-	-	-16	-	dB
C/I 2 MHz adjacent channel	-	-	-34	-	dB
C/I -2 MHz adjacent channel	-	-	-40	-	dB
C/I 3 MHz adjacent channel	-	-	-42	-	dB
C/I -3 MHz adjacent channel	-	-	-43	-	dB
C/I > 3 MHz adjacent channel	-	-	-41	-	dB
C/I < -3 MHz adjacent channel	-	-	-42	-	dB
Bluetooth LE 500 kbps					
Sensitivity	30.8% PER	-	-99	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	5	-	dB
C/I 1 MHz adjacent channel	-	-	-2	-	dB
C/I -1 MHz adjacent channel	-	-	-3	-	dB
C/I 2 MHz adjacent channel	-	-	-30	-	dB
C/I -2 MHz adjacent channel	-	-	-31	-	dB
C/I 3 MHz adjacent channel	-	-	-31	-	dB
C/I -3 MHz adjacent channel	-	-	-40	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I > 3 MHz adjacent channel	-	-	-36	-	dB
C/I < -3 MHz adjacent channel	-	-	-36	-	dB

5.15 Bluetooth LE RF Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter		Condition	Min.	Typ.	Max.	Unit
General						
Frequency range		-	2402	-	2480	MHz
TX power		-	-20	6	15	dBm
Bluetooth LE 1 Mbps						
In-band emissions	±2 MHz offset	-	-	-47	-	dBm
	±3 MHz offset	-	-	-49	-	dBm
	>±3 MHz offset	-	-	-50	-	dBm
Modulation characteristics	Δf1avg	-	225	245	275	kHz
	Δf2max	-	185	235	-	kHz
	Δf2avg/Δf1avg	-	0.8	0.93	-	-
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	3	150	kHz
	Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	2.5	50	kHz
	$\|f_1 - f_0\|$	-	-	2	23	kHz
	Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	2.5	20	kHz/50 μs
Bluetooth LE 2 Mbps						
In-band emissions	±4 MHz offset	-	-	-50	-	dBm
	±5 MHz offset	-	-	-51	-	dBm
	>±5 MHz offset	-	-	-52	-	dBm
Modulation characteristics	Δf1avg	-	-	488	-	kHz
	Δf2max	-	-	469	-	kHz
	Δf2avg/Δf1avg	-	-	0.93	-	-

Parameter		Condition	Min.	Typ.	Max.	Unit
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	3	150	kHz
	Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	2.5	50	kHz
	$\|f_1 - f_0\|$	-	-	1.5	23	kHz
	Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	2.5	20	kHz/50 μs
Bluetooth LE 125 kbps						
In-band emissions	±2 MHz offset	-	-	-47	-	dBm
	±3 MHz offset	-	-	-49	-	dBm
	>±3 MHz offset	-	-	-50	-	dBm
Modulation characteristics	Δf1avg	-	225	245	275	kHz
	Δf1max	-	185	246	-	kHz
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	1.5	150	kHz
	Max $\|f_0 - f_n\|$ n = 1, 2, 3…k	-	-	1.5	50	kHz
	$\|f_0 - f_3\|$	-	-	1.5	19.2	kHz
	$\|f_n - f_{n-3}\|$ n = 7, 8, 9…k	-	-	1.5	19.2	kHz/48 μs
Bluetooth LE 500 kbps						
In-band emissions	±2 MHz offset	-	-	-47	-	dBm
	±3 MHz offset	-	-	-49	-	dBm
	>±3 MHz offset	-	-	-50	-	dBm

5.16 Audio Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
DAC differential output	With 600 Ω load	-	1	-	Vrms
	With 16 Ω load	-	0.8	-	Vrms
DAC differential output THD	With 0.7 Vrms @ 600 Ω load	-	-	-80	dB
	With 0.65 Vrms @ 16 Ω load	-	-	-80	dB
DAC output SNR	1 kHz sine wave	-	104	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
DAC sampling rate	-	8	-	48	kHz
ADC SNR	1 kHz sine wave	-	100	-	dB
ADC sampling rate	-	8	-	48	kHz

5.17 AUX ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Conversion clock	-	0.2	-	13	MHz
Conversion time	-	-	16	-	Cycle
V_{REF}	Internal	-	1.1	-	V
	External	-	VIO/3	-	V
Input voltage range	-	0	-	V_{REF}*N(1)	V
Input impedance	-	10	-	-	MΩ
Input capacitance (Cs)	-	-	1	-	pF
DNL	-	-1	-	3	LSB
INL	-	-5	-	5	LSB
ENOB	-	-	10	-	Bit
SNDR	-	-	62	-	dB
SFDR	-	-	77	-	dB
$T_{STARTUP}$	-	-	5	-	μs
Current consumption	-	-	200	-	μA

(1) N is the input voltage division factor. N=1, 2, 3, or 4.

6. Package Information

Figure 6-1 QFN56 7 x 7 mm Package Outline

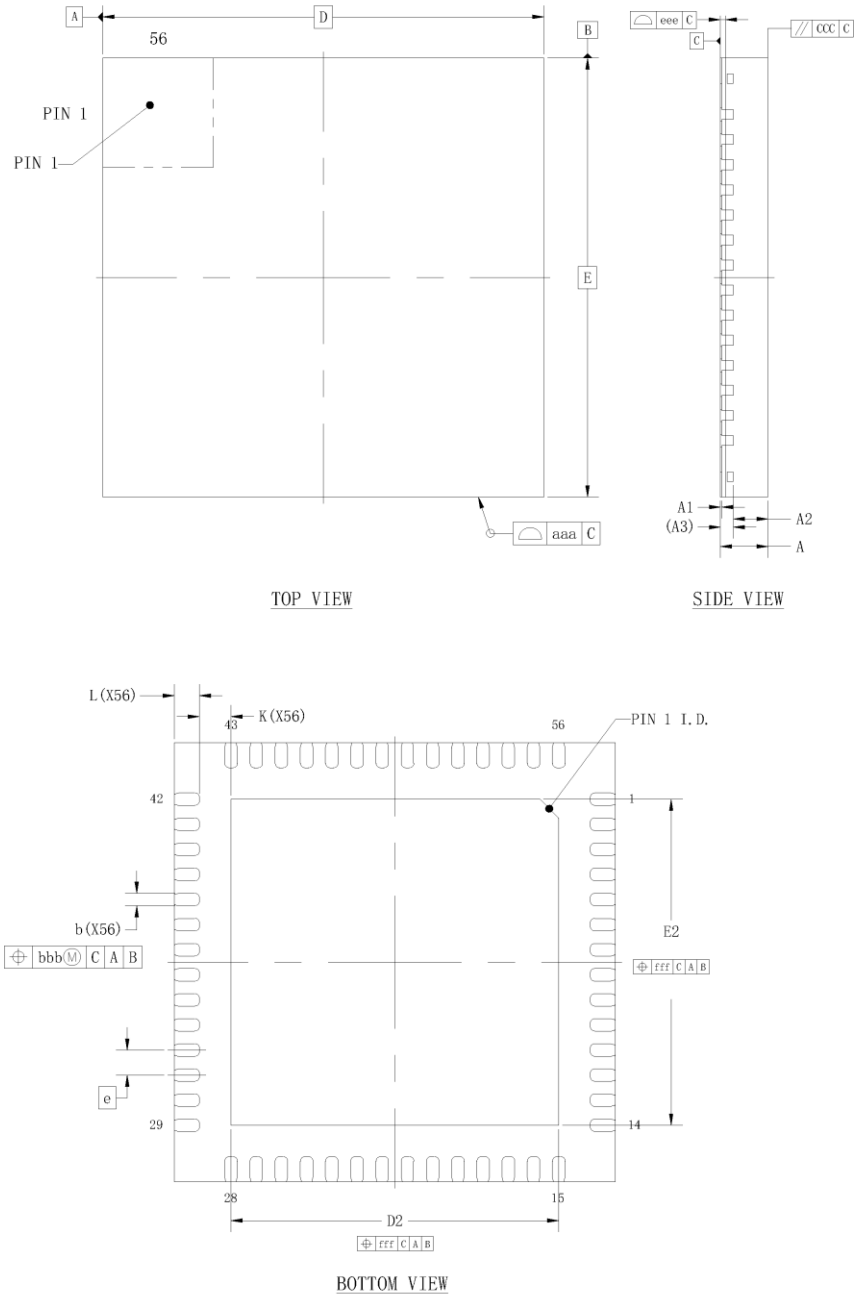
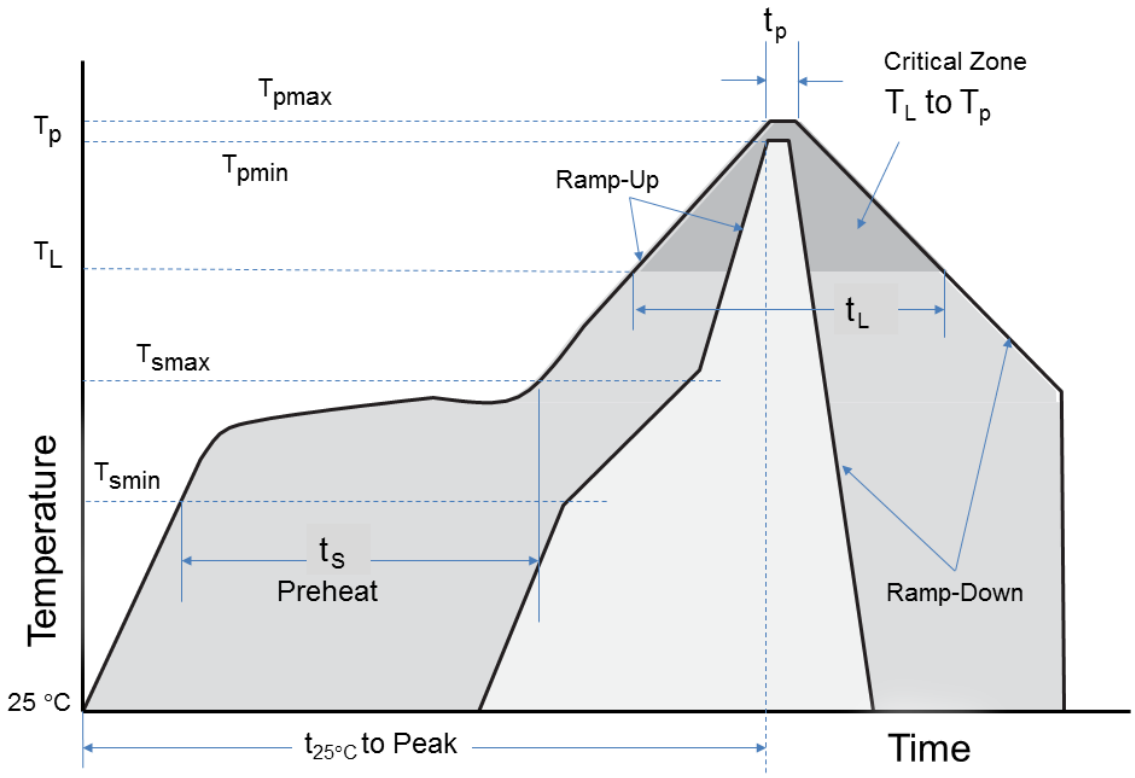


Table 6-1 QFN56 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	-	0.55	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	7.00 BSC		
E	7.00 BSC		
e	0.40 BSC		
D2	5.10	5.20	5.30
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
K	0.50 REF		
aaa	0.10		
ccc	0.10		
eee	0.08		
bbb	0.07		
fff	0.10		

7. Reflow Soldering Profile

Figure 7-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 ℃/s max.
Preheat	Temperature min. (T_{smin})	150 ℃
	Temperature max. (T_{smax})	200 ℃
	Time (t_s)	60 s to 180 s
Time maintained above	Temperature (T_L)	217 ℃
	Time (t_L)	60 s to 150 s
Peak/classification temperature (T_p)		260 ℃
Time within 5 ℃ of actual peak temperature (t_p)		20 s to 40 s

Profile Feature	Specification
Ramp-down rate	6 ℃/s max.
Time 25 ℃ to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, or DIBP content in accordance with EU RoHS Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

8. Ordering Information

Figure 8-1 Ordering Code Scheme

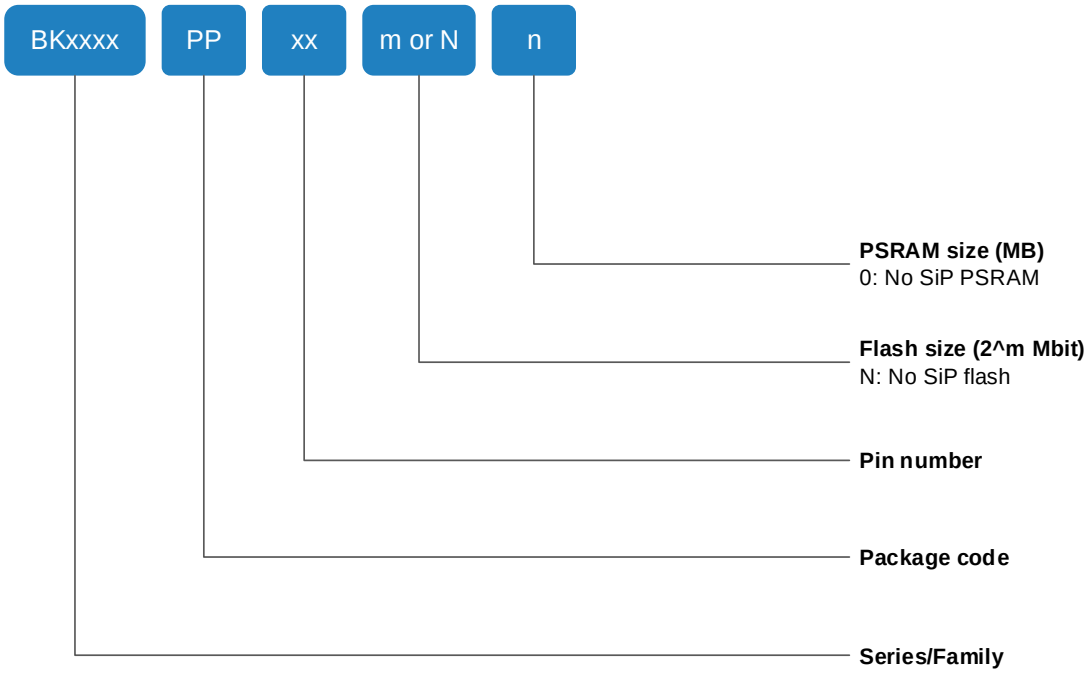


Table 8-1 Ordering Information

Ordering Code	Package	SiP(1) Flash	SiP PSRAM	Packing	Minimum Ordering Qty (MOQ)(2)
BK7257QN5650	7 mm x 7 mm QFN56	4 MB	-	Tape and Reel	3000
BK7257QN5660	7 mm x 7 mm QFN56	8 MB	-	Tape and Reel	3000

(1) A system in a package (SiP) refers to flash/PSRAM enclosed in the package.

(2) The MOQ for customized or exclusive ordering codes is one wafer lot. Please consult your sales representative for the exact quantity.

Revision History

Version	Date	Description
1.0	2025/5/9	Initial release

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